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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,162	12/15/2003	Ji Yong Park	0095.1054	2087

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EXAMINER	
KIM, JAY C	

ART UNIT	PAPER NUMBER
2815	

NOTIFICATION DATE	DELIVERY MODE
12/02/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

usptomail@smiplaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/734,162	PARK ET AL.	
	Examiner	Art Unit	
	JAY C. KIM	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-7 and 9-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7 and 9-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to Amendment filed October 22, 2010.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 6, 7 and 9-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Oka et al. (US 6,184,541).

Regarding claim 6, Oka et al. disclose a thin film transistor (TFT) (Figs. 1(a), 1(b) and 3(g)) comprising a channel region (8) (col. 3, line 42), source and drain regions (5) (col. 3, lines 39-40) respectively formed at opposite sides (left and right sides) of the channel region (8), lightly doped drain (LDD) or offset regions (portions of regions 4 having a width *d* in Fig. 1(b)) (col. 3, lines 60-66, and col. 4, lines 63-66) formed at respective opposite sides (left and right sides) of the channel region (8) and between the source and drain regions (5), and a plurality of primary crystal grain boundaries (2 along vertical directions in Figs. 1(a), 1(b) and 3(g)) (col. 3, lines 36-37), wherein the thin film transistor is formed so that the primary crystal grain boundaries (2) of a polysilicon substrate (3) (col. 3, line 36) are positioned in the channel, source and drain regions (8 and 5) but not positioned in the LDD or offset regions (portions of regions 4 having a width *d* in Fig. 1(b)), and wherein a width (*d*) of the LDD or offset regions is

less than a distance between two adjoining primary crystal grain boundaries (one rightmost primary crystal grain boundary in channel region 8 and another leftmost primary crystal grain boundary in region 4 on the right shown in Fig. 1(a)) because the LDD or offset regions are formed between two adjoining primary crystal grain boundaries.

Regarding claim 7, Oka et al. disclose a flat panel display device (col. 2, lines 27-29) comprising a thin film transistor (TFT) (Figs. 1(a), 1(b) and 3(g)) comprising a channel region (8) (col. 3, line 42), offset regions or *off-center regions* (portions of regions 4 having a width *d* in Fig. 1(b)) (col. 3, lines 38-39) formed at opposite sides (left and right sides) of the channel region (8), source and drain regions (5) (col. 3, lines 39-40) respectively formed at outer sides of the offset regions, and a plurality of primary crystal grain boundaries (2 along vertical directions in Figs. 1(a), 1(b) and 3(g)) (col. 3, lines 36-37), wherein the thin film transistor is formed so that the primary crystal grain boundaries (2) of a polysilicon substrate (3) (col. 3, line 36) are not positioned in the offset regions (portions of regions 4 having a width *d* in Fig. 1(b)), and wherein a width of the offset regions (*d*) is smaller than a distance between the primary crystal grain boundaries (2) because the offset regions are formed between two primary crystal grain boundaries, for example, one rightmost primary crystal grain boundary in channel region 8 and another leftmost primary crystal grain boundary in region 4 on the right shown in Fig. 1(a).

Regarding claim 9, Oka et al. disclose the flat panel display device according to claim 7.

The limitation "the polysilicon substrate is formed by a sequential lateral solidification (SLS) method" is merely a product-by-process limitation that does not structurally distinguish the claimed invention over the prior art. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. *In re Thorpe*, 227 USPQ 964, 966.

Regarding claim 10, Oka et al. further disclose for the flat panel display device according to claim 7 that the thin film transistor is used in an LCD device (col. 2, lines 27-29).

Regarding claim 11, Oka et al. further disclose for the flat panel display device according to claim 7 that the primary crystal grain boundaries (2 along vertical directions in Figs. 1(a), 1(b) and 3(g)) are substantially perpendicular to a current direction (left-to-right or right-to-left direction) between the source and drain regions (5) of the thin film transistor.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 and 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oka et al. (US 6,184,541).

Regarding claim 1, Oka et al. disclose a thin film transistor (TFT) (Figs. 1(a), 1(b) and 3(g)) comprising a channel region (8) (col. 3, line 42) having a plurality of primary crystal grain boundaries (2) (col. 3, lines 36-37), source and drain regions (5) (col. 3, lines 39-40) formed at respective ends (left and right ends) of the channel region (8), and offset regions or *off-center regions* (portions of regions 4 having a width *d* in Fig. 1(b)) (col. 3, lines 38-39) one of which is formed between the channel region (8) and the source region (5) and the other of which is formed between the channel region (8) and the drain region (5), wherein the thin film transistor is formed so that the primary crystal grain boundaries (2 along vertical directions in Figs. 1(a), 1(b) and 3(g)) of a polysilicon substrate (3) (col. 3, line 36) are not positioned in the offset regions (portions of regions 4 having a width *d* in Fig. 1(b)).

Oka et al. differ from the claimed invention by not showing that a width of each one of the offset regions is smaller than a distance between the primary crystal grain boundaries formed in the channel region.

Oka et al. further disclose that the grain size of the polysilicon substrate (16 in Fig. 3(b)) is as fine as 1.0 ± 0.5 μm and the polysilicon substrate itself has high homogeneity (col. 4, lines 40-41).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that a width of each one of the offset regions (*d*) may be smaller than a distance between the primary crystal grain boundaries formed in the

channel region, because *d* is smaller than a lateral grain size of polysilicon grains in which an offset region is formed, and the width of each one of the offset regions (*d*) may be smaller than a distance between primary crystal grain boundaries (distance between nearest neighboring primary crystal grain boundaries, or distance between next nearest neighboring primary crystal grain boundaries) formed in the channel region when the grain size of the polysilicon substrate is substantially uniform.

Regarding claim 3, Oka et al. disclose the thin film transistor according to claim 1.

The limitation "the polysilicon substrate is formed by a sequential lateral solidification (SLS) method" is merely a product-by-process limitation that does not structurally distinguish the claimed invention over the prior art. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. *In re Thorpe*, 227 USPQ 964, 966.

Regarding claim 4, Oka et al. further disclose for the thin film transistor according to claim 1 that the thin film transistor is used in an LCD device (col. 2, lines 27-29).

Regarding claim 5, Oka et al. further disclose for the thin film transistor according to claim 1 that the primary crystal grain boundaries (2 along vertical directions in Figs. 1(a), 1(b) and 3(g)) are substantially perpendicular to a current direction (left-to-right or right-to-left direction) between the source and drain regions (5) of the thin film transistor.

Response to Arguments

5. Applicants' arguments filed October 22, 2010 have been fully considered but they are not persuasive.

Applicants argue that "however, Applicants note that Oka teaches that when the grain size is longer than the length "D" of the low concentration region, the high concentration impurity diffuses deeply along the grain boundary, thereby shortening an effective length "d" of the low concentration region", that "accordingly, Oka teaches away from forming the width of the LDD or offset regions to be less than a distance between two adjoining primary crystal grain boundaries, since such formation would produce a leakage current", that "in essence, Oka maintains the length of the low concentration region to be "D," and thus the offset or LDD region is "D" and not "d" as noted by the Examiner", that "accordingly, the primary crystal grain boundaries of the polysilicon substrate are positioned in the LDD or offset regions, contrary to the recitation of independent claim 6", and that "therefore, since Oka clearly teaches that the LDD or offset region is "D" Applicants respectfully note that there is no basis in the reference to specify that the effective length is "d," as suggested by the Examiner". These arguments are not convincing because: (1) Claims must be given their broadest reasonable interpretation, see MPEP 2111, and therefore Applicants cannot suggest that the Examiner should interpret the prior art in a certain way when an alternate reasonable interpretation is also possible, (2) Applicants do not specifically claim a structure or positional relationship of the LDD or offset regions or whether the recited LDD or offset regions are whole LDD or offset regions in physical contact with the

channel region and/or the source/drain region, (3) Applicants' definition of LDD or offset regions is unduly narrow without specifically claiming a structure or positional relationship of the LDD or offset regions, (4) a portion of region 4 having a width *d* in Fig. 1(b) of Oka et al. can be reasonably referred to as an LDD or offset region, while a whole region 4 may also be reasonably referred to as an LDD or offset region, because both of them have distinct structures distinguished from surroundings; in the former case, the rest of region 4 adjacent to the portion of region 4 having a width *d* can be referred to as another LDD region or offset region, (5) Fig. 6 of current Application shows a width of LDD or offset regions II is smaller than a distance between the channel region having a width I and source/drain regions 13a, which suggests that Applicants' disclosed structure may have another LDD or offset regions between the LDD or offset regions having a width II and the source/drain regions 13a, i.e. Applicants' claimed LDD or offset regions may not be whole LDD or offset regions, either, (6) the arguments above may be based on importing claim limitations from the specification, which is improper according to MPEP 2111.01, and (7) it is not clear what Applicants suggest by "the effective length", which is not disclosed or claimed by Applicants.

Conclusion

6. Applicants' amendment necessitated the new ground of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAY C. KIM whose telephone number is (571)270-1620. The examiner can normally be reached on 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. K./
Examiner, Art Unit 2815
November 24, 2010

/Jerome Jackson Jr./
Primary Examiner, Art Unit 2815